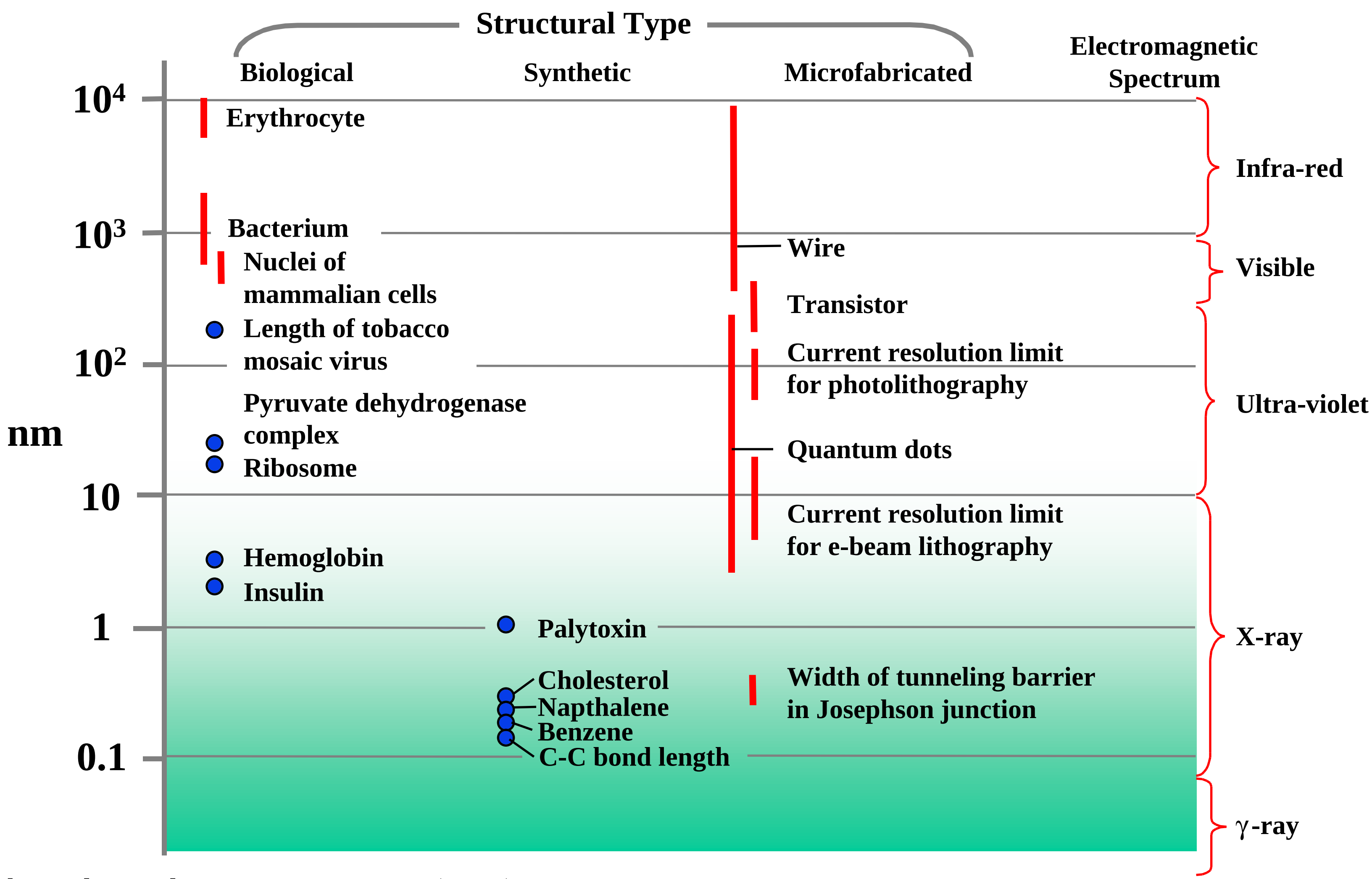
E298A/EE290B
Introduction to Electron Beam Lithography & Nanofabrication Technology

Erik H. Anderson & J. Alexander Liddle

Materials Sciences Division, Lawrence Berkeley National Laboratory

Lectures: Tuesdays, 2:00 pm – 3:30 pm
71 Evans Hall, UC Campus
Lab: Thursdays 3:00 pm – 5:00 pm
Bldg. 2, Rm. 137, LBL

The Scale of Things



After Whitesides et al. *Science*, **254** 1312 (1992)

Contact Information

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- Alexander Liddle
  - 510 486 5260
  - Jaliddle@lbl.gov
- Lab, LBL Building 2 room 137
  - 510 486 4332

Course Details

- *Homework:* Weekly assignments due at the beginning of the Thursday lab session
- *Report:* A written term paper will be required. An experimental project will be required. An oral presentation of paper to class will be required.
- *Grading:* Grades will be based on the weekly homework and term paper
  - Homework – 30%
  - Project Proposal – 20%
  - Project Report – 40%
  - Project Presentation – 10%

Expectations

- Homework
  - Handed out at Tuesday classes, due at start of the lab session on the following Thursday.
  - Assume access to Mathematica, MatLab etc.
- Lab
  - Starts *promptly* at 3:00 pm
  - Shuttle buses run approx. every 10 mins
  - Passes required - will be e-mailed
- Lectures
  - Interactive!

Project Guidelines I

- A project is required for the class and is expected to be a substantial part of the learning experience. The scope of the project should be realistic and take into account the limitations in time and materials. The project should explore a scientific application where electron beam lithography is need to achieve a result, or the electron beam lithographic process itself. The project will consist of a written proposal, which must describe the planned experiments together with a suitable schedule. The proposals will be reviewed to make sure that the scope is appropriate. The project milestones are expected to be followed. A written report of the project results and a formal presentation to the class are required.
- Proposals due Tuesday, February 17^{th} - we will review the proposals individually on February 12^{th}
- The report is due Tuesday, May 4^{th}
  - The report should be formatted in the style of a JVST paper, 4-6 pages in length. Each journal page is approx. 900 words, and each figure is equivalent to 200 words
- Class presentations will be on Thursday May 6^{th}, which will be the last day of class. Each presentation will be 15 minutes long in the style of a conference talk.
  - Allow 1 minute per viewgraph and 2 minutes for questions

Project Guidelines II

- The work at LBL will be under the supervision of E.H. Anderson and J.A. Liddle
- The project can be related to the thesis work of the student, but should not be in the critical path!
- The project should use readily available materials and processes to the fullest extent possible. Health and safety issues may restrict materials and processes – investigate these possibilities early
- Samples for e-beam lithography can be on 3 – 8" wafers and quartz plates. No fragments!
- Data sets can be generated at LBL or with any CAD system that produces a suitable GDSII file
- Start prototyping and process development early!
- Plan something that will be instructive *and* fun

Project Hints

- The voice of experience….
  - How hard could it be….?
  - What could possibly go wrong….?
- Keep the project scope simple, focused and reasonable. Estimate what you think you can do, and divide by two, focusing on the critical elements. This is a class project and not a thesis!
- Start early! Experimental efforts always take longer than expected, even when you know that experimental efforts always take longer than expected (yes, this is recursive!). Lots of things can go wrong in the lab, and often do. Remember, if you can't imagine how something could fail, it just shows a lack of imagination!
- Don't reinvent the wheel – if someone has already gone to the trouble of developing a process, use it!
- The written proposal is only a plan and *"no plan survives contact with the enemy"*. Be prepared to update your plan in light of experience.

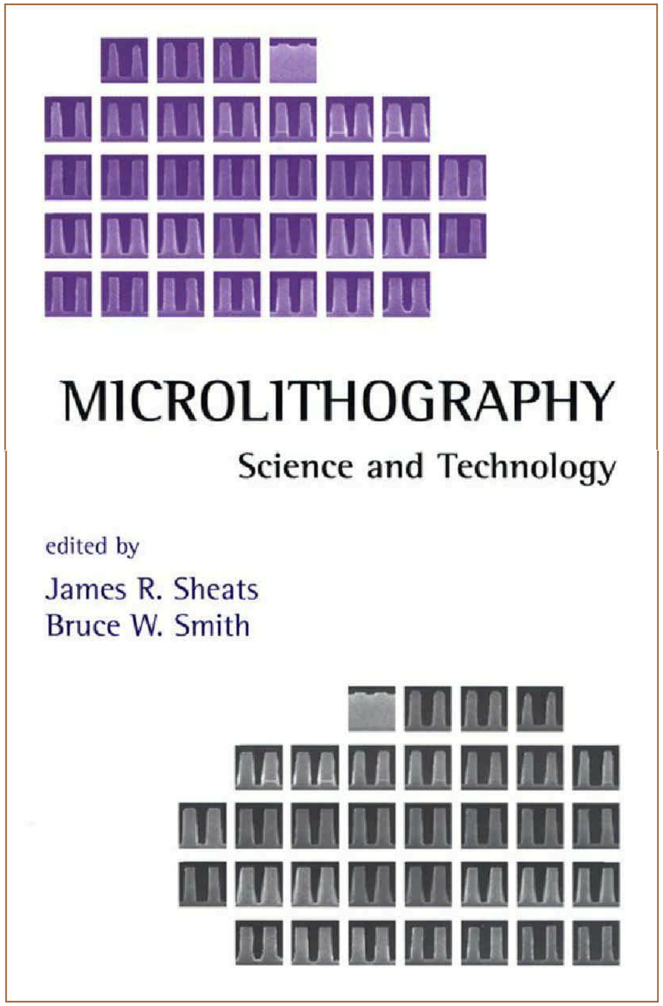
Course Outline

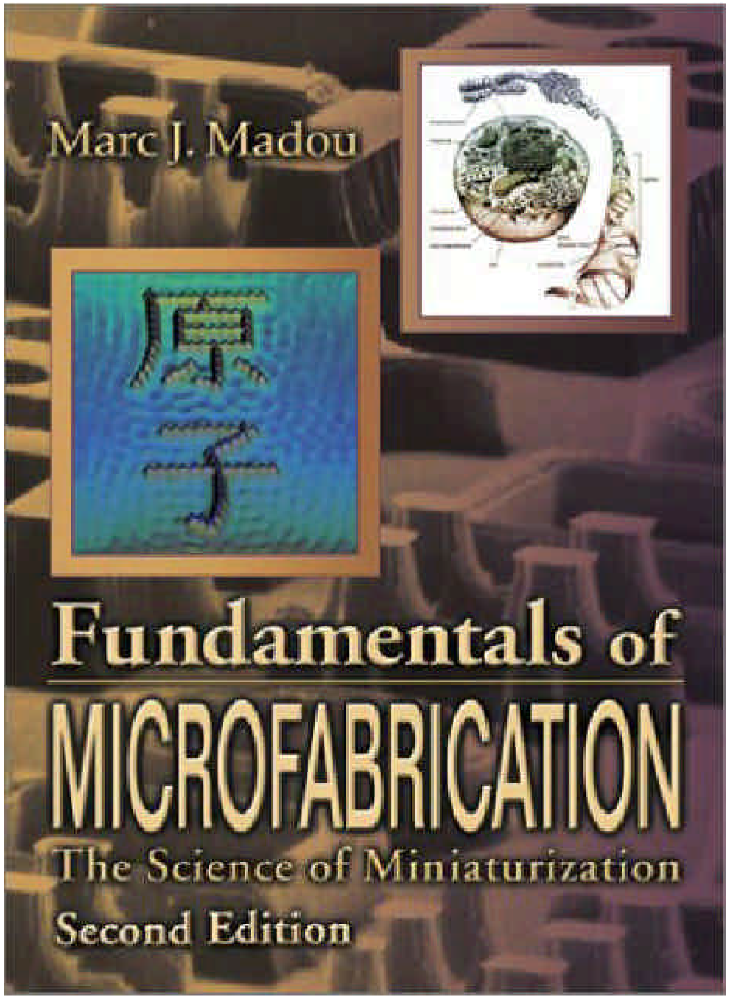
- Introduction - EHA/JAL
- Patterning Technology - JAL
- Fundamentals of E-Beam Systems I - EHA
- Data Fracturing and Processing - EHA
- Electron Interactions in Solids - JAL
- Fundamentals of E-Beam Systems II - EHA
- Nanofabrication Characterization I - JAL

Course Outline

- Resist Materials I - JAL
- Resist Materials II - JAL
- Proximity Effect and Correction - EHA
- Pattern Transfer Techniques I - JAL
- E-Beam Writing Strategies - EHA
- Project Presentations

Recommended Textbooks





Suggested Reading

- *Microlithography, Micromachining and Microfabrication* – P. Rai-Choudhury
- *Introduction to Microlithography* – L.F. Thompson, C.G. Willson and M.J. Bowden
- *Microsystem Design* – Stephen D. Senturia
- *Scanning Electron Microscopy* – Ludwig Reimer
- *Micro-Optics* – Hans Peter Herzig, Ed.
- *Signs of Life* – Ricard Solé & Brian Goodwin
- *The Diamond Age* – Neal Stephenson

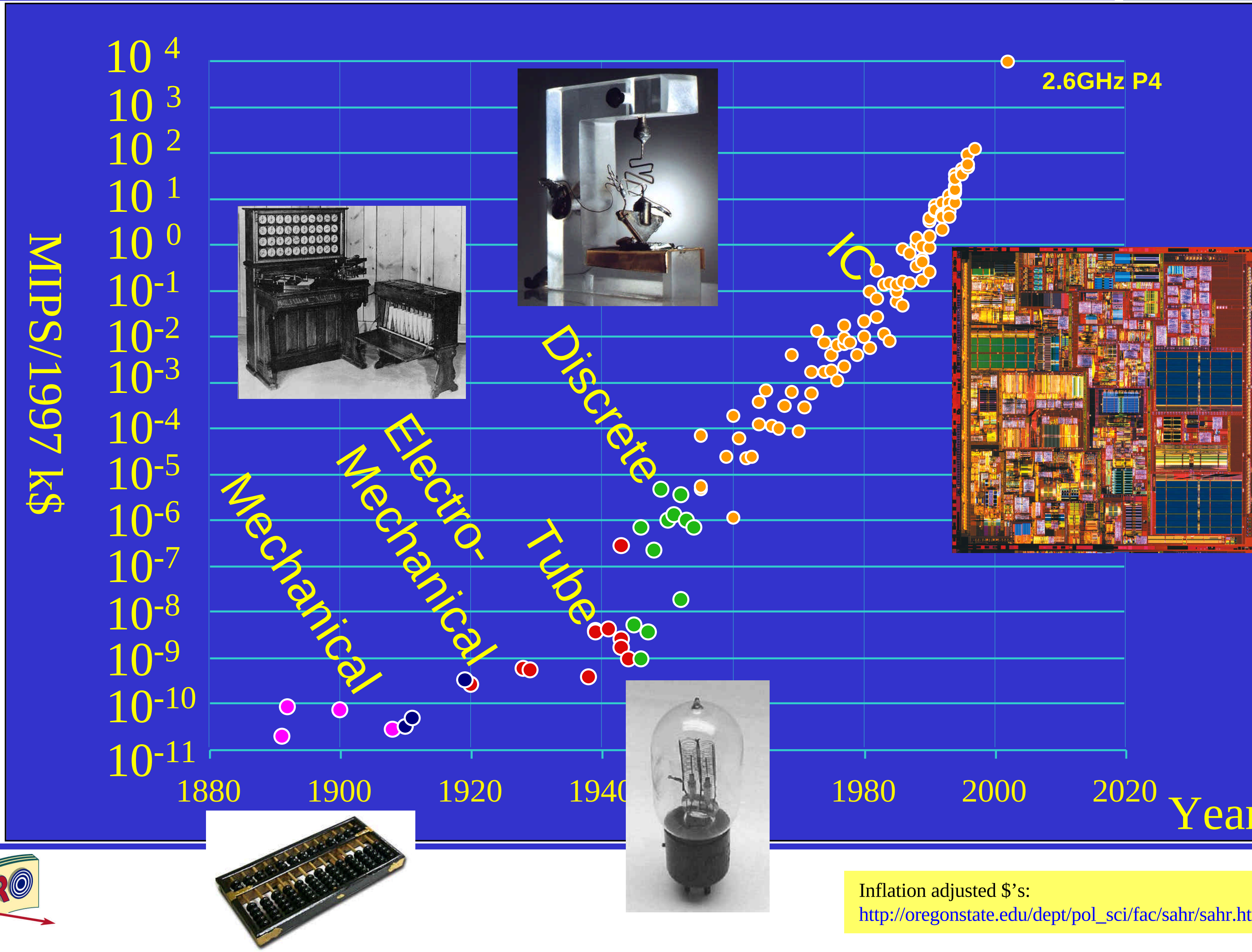
After Taking This Course….

- You should have a basic understanding of the complete sequence in the nanofabrication process from CAD through to fabricated structure including basic metrology and characterization
- You will have completed a project and presented it professionally to your peers
- You should be familiar with the current state-of-the-art and inspired to improve it!

2003 Class Projects

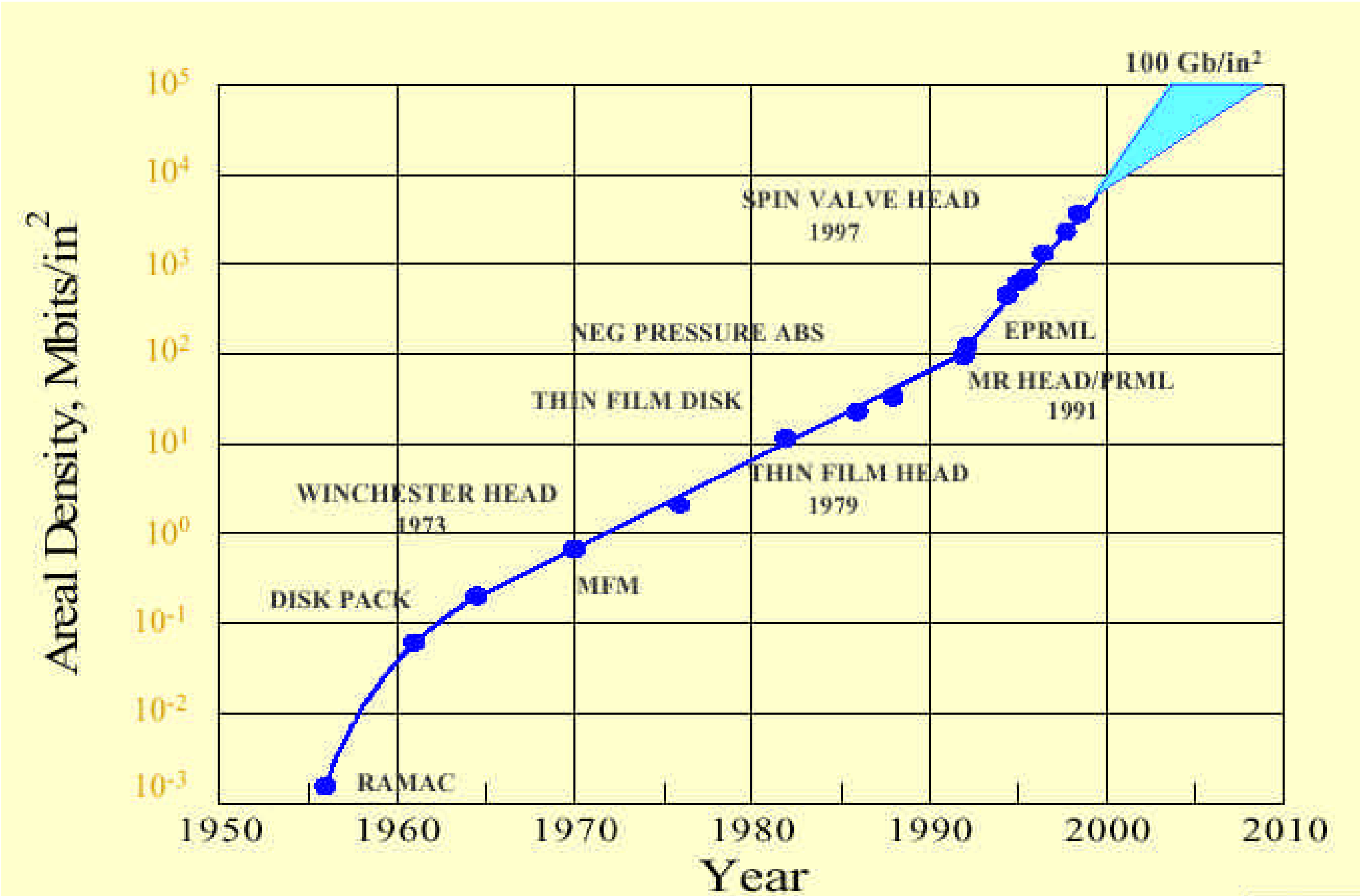
Daewon Ha:-	*Impact of Alignment-Mark on Statistical Alignment Accuracy in E-beam lithography* (Paper at MNE2003)
Garth Robins:-	*Pattern and Probe-based Aberration Monitors for the Human Eye*
Gregory McIntyre:-	*Direct-Write of Phase-Shifting Mask to Characterize Optical Lithography Illumination*
Jeremy Robinson:-	*Nanocatalyst Fabrication Using a Stencil Mask* (LDRD 2003)
Kyoungsub Shin:-	*Process Optimization for AZPN/HSQ Bilayer Resist E-Beam Lithography: Effects of PAB and Development Time*
Varadarajan Vidya:-	*Sub-20 nm Gate Definition for MESFET/MOSFET IC Applications*
Sriram Balasubramanian:-	*Application of E-beam Lithography to FinFET Based SRAMs*
Yu-Chih Tseng:-	*High Energy Electron Beam Lithography on Self-Assembled Monolayer of 3-aminopropyltriethoxysilane*

Cost of Computing Power Versus Time



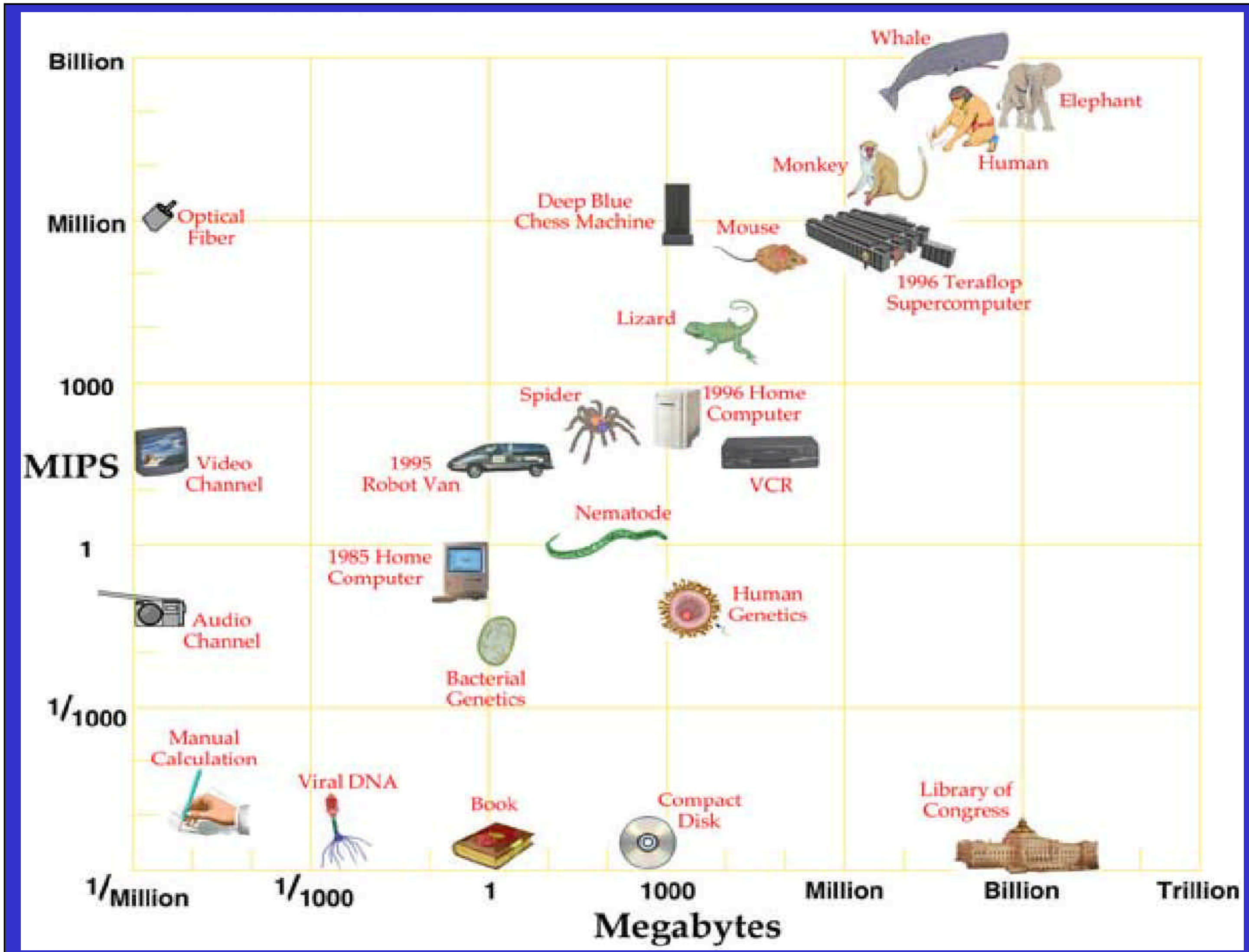
Inflation adjusted $'s:
http://oregonstate.edu/dept/pol_sci/fac/sahr/sahr.htm

Storage Capacity vs Time



David B. Bogy, UCB

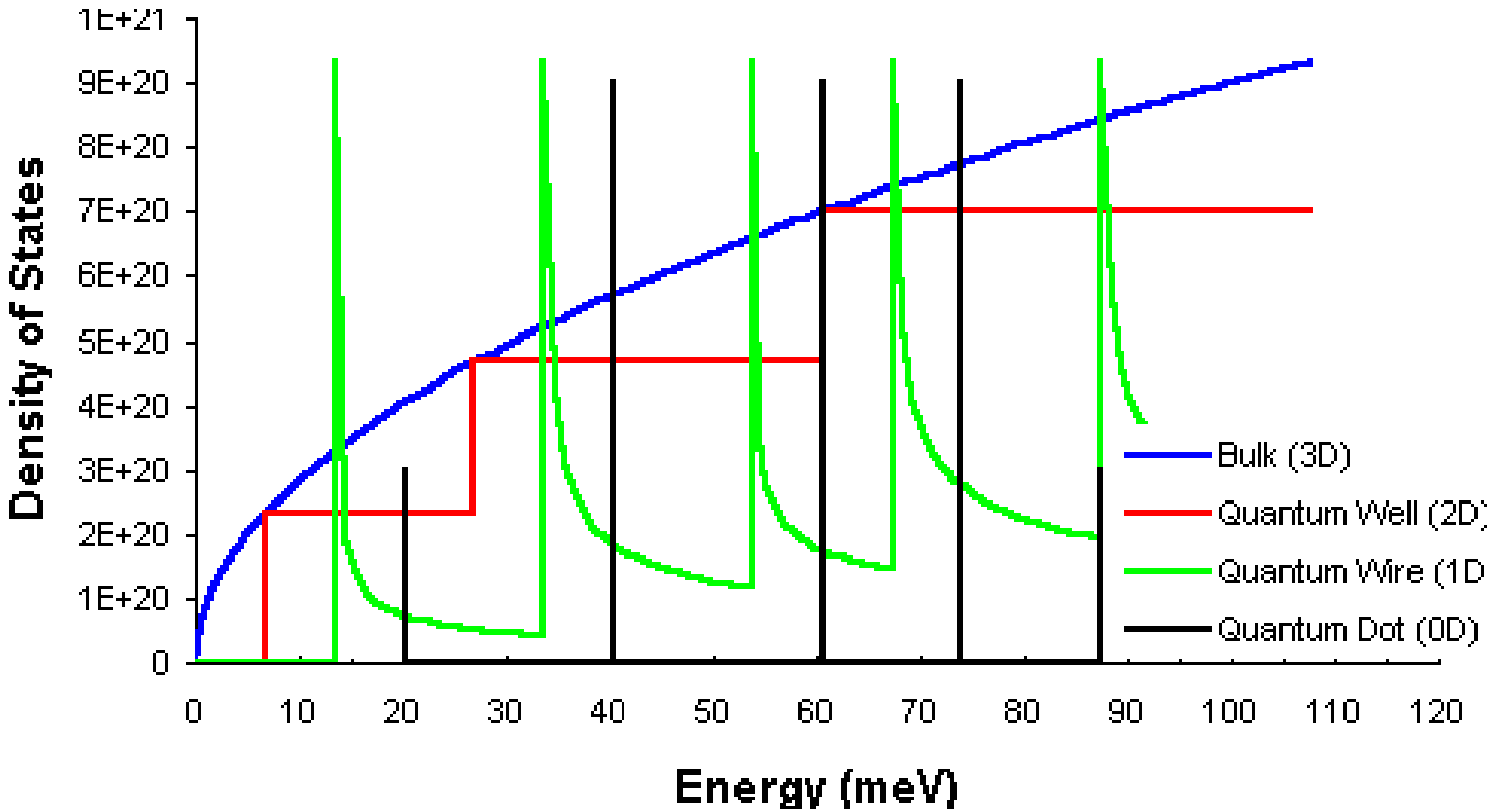
Evolution of Computational Power



Hans Moravec, Journal of Evolution and Technology. 1998. Vol. 1

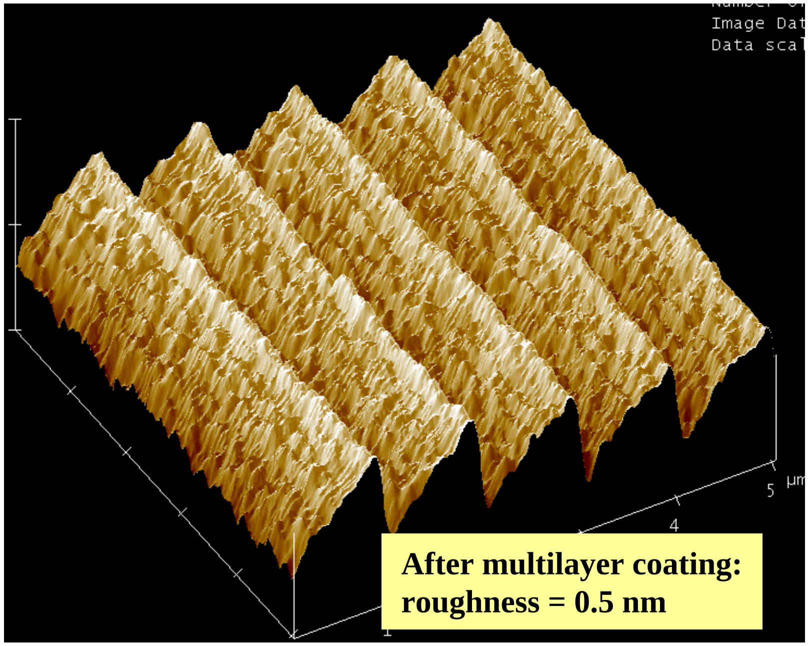
http://www.transhumanist.com/volume1/moravec.htm

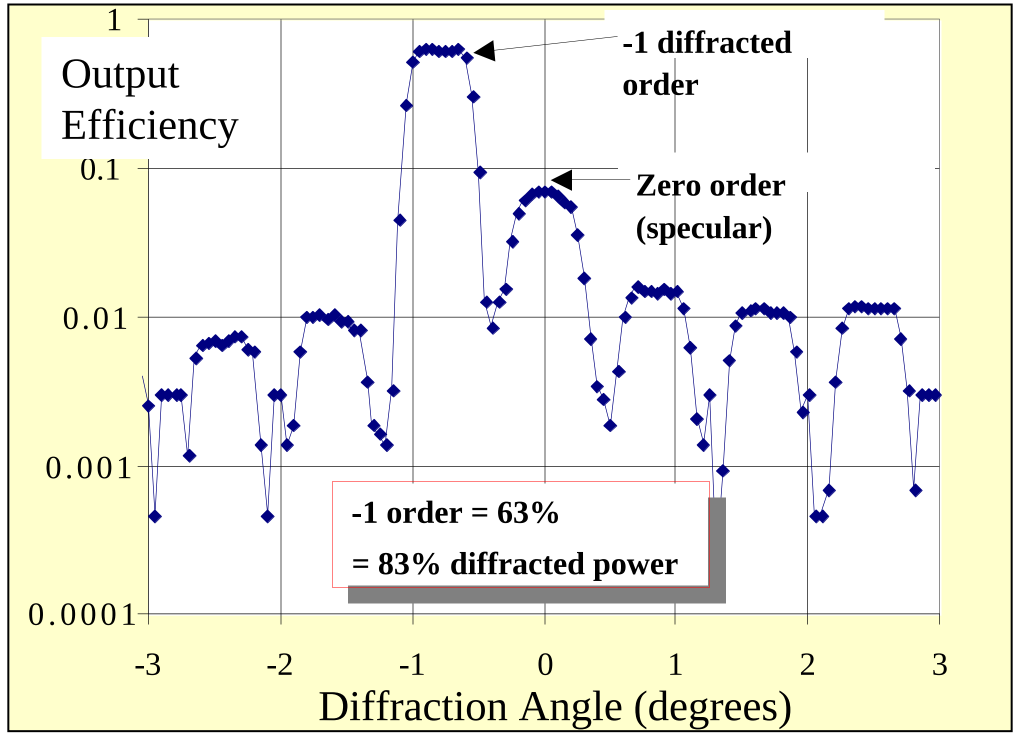
Effect of Dimensionality on DoS

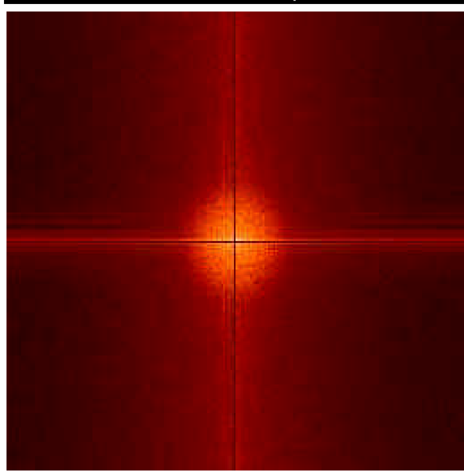


http://britneyspears.ac/physics/dos/dos.htm
http://britneyspears.ac/lasers.htm

EUV Blazed Grating

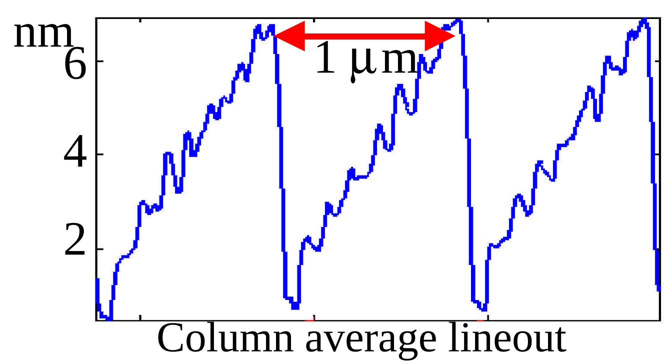




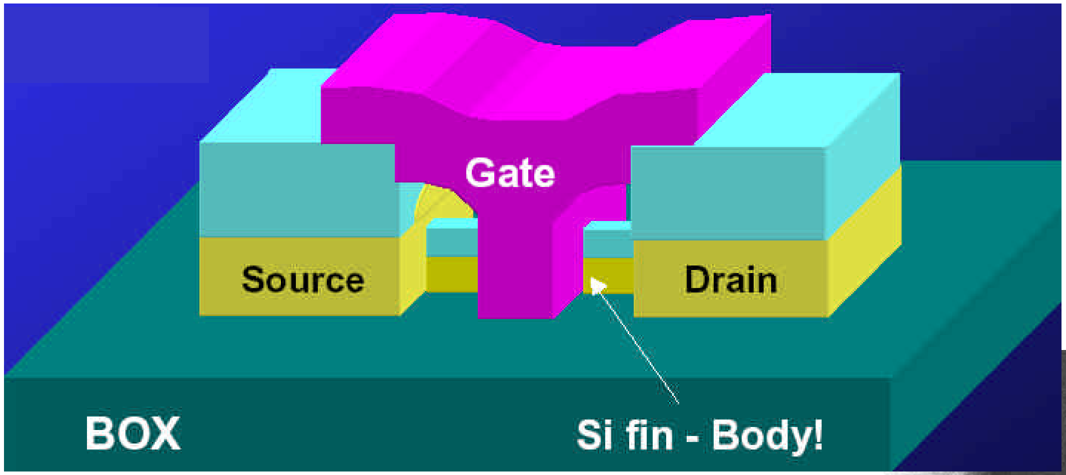


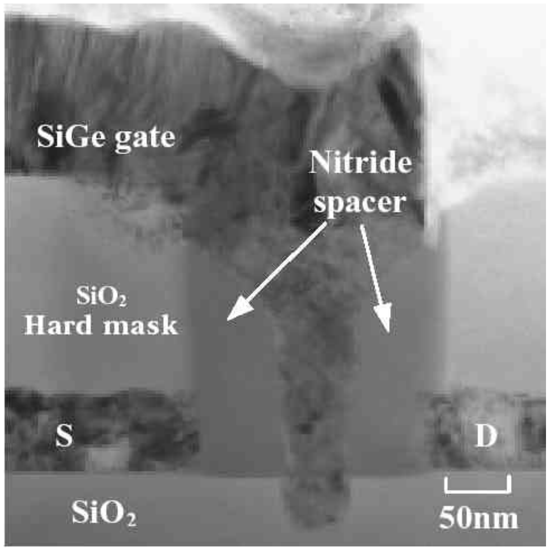
Light is scattered by surface roughness – loss in diffracted power

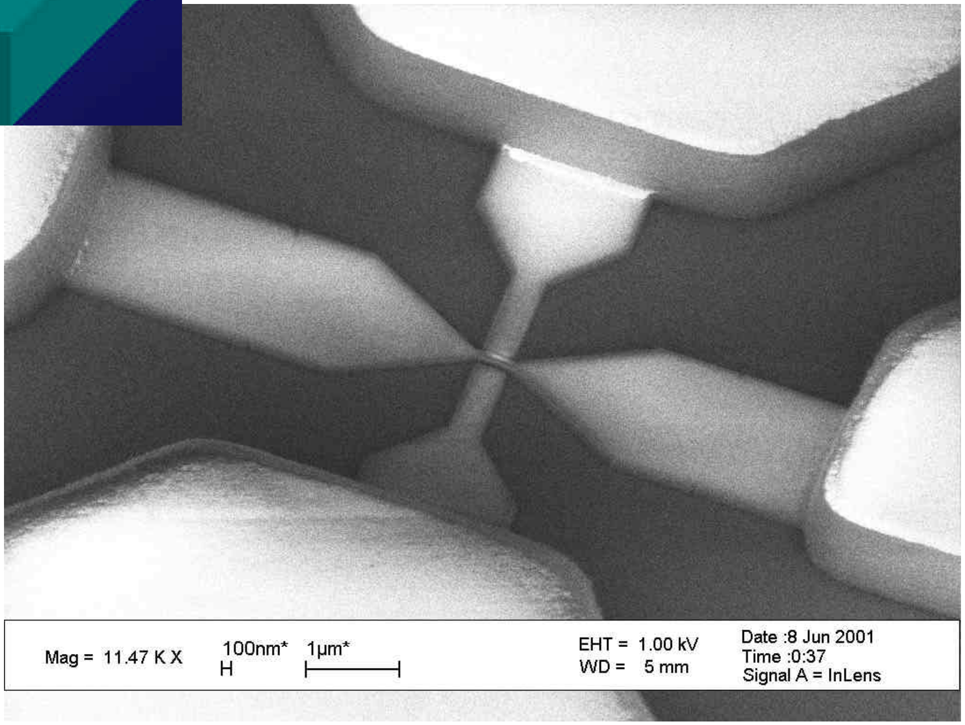
⇐ PSD of multilayer coated grating



Nano-electronics LBNL/UC Berkeley





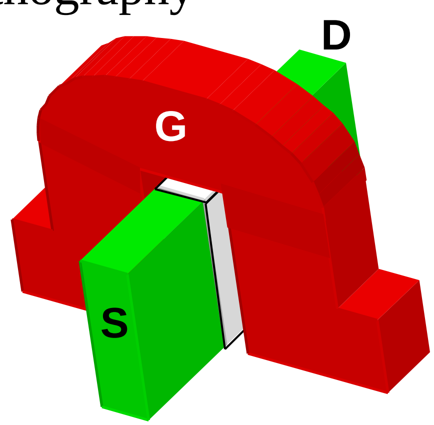


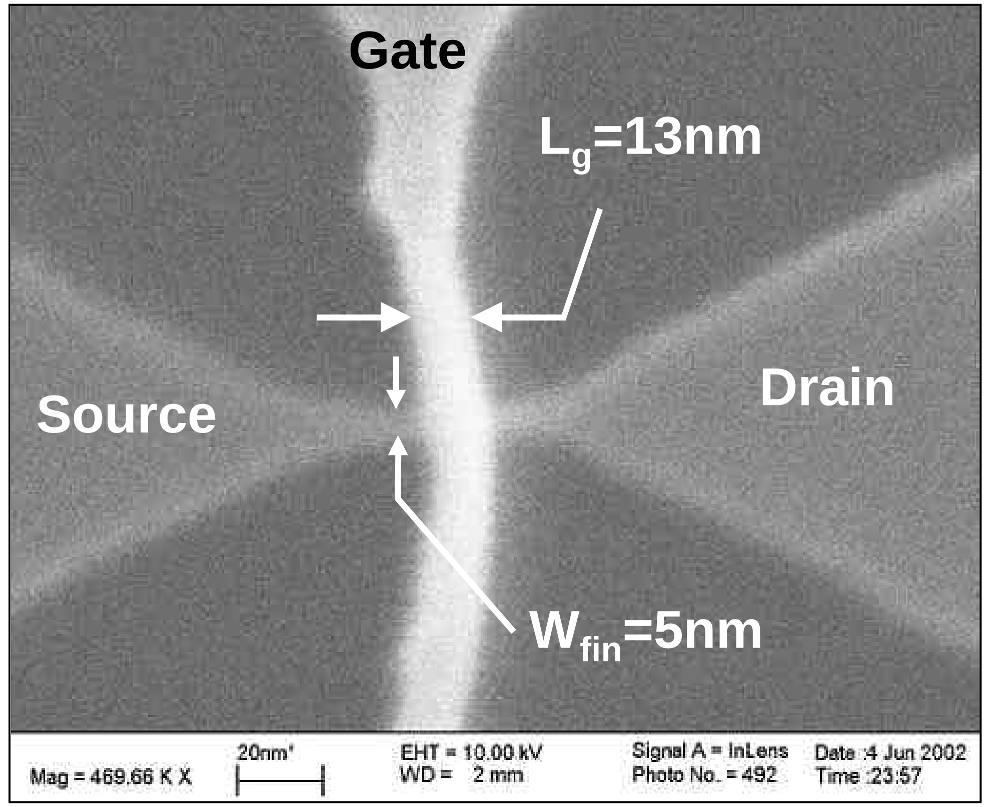
X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub-50 nm FinFET: PMOS," IEEE IEDM Technical Digest,

FinFET Fabrication

What is the ultimate limit of CMOS devices?

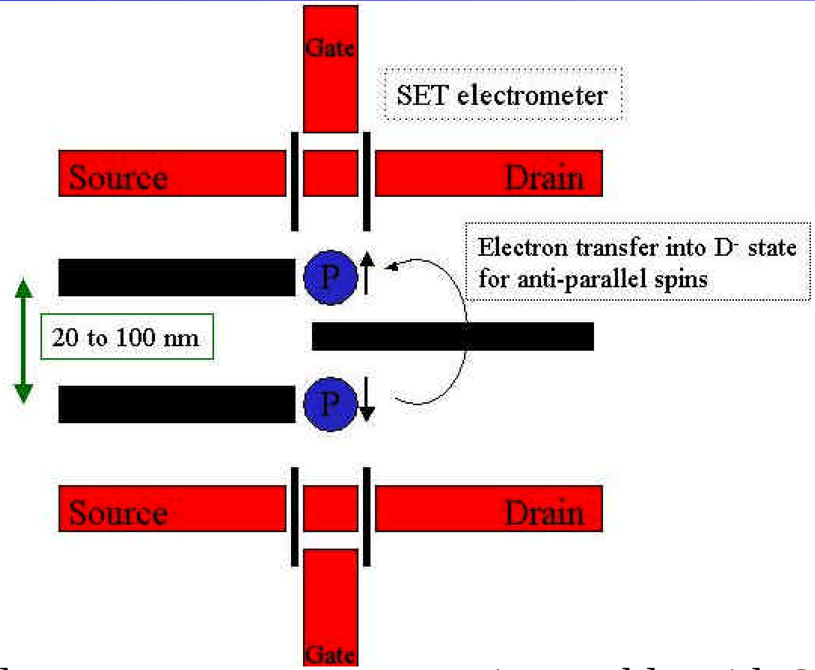
- FinFET is the most promising device structure for deep sub 100 nm device operation
  - Gate lengths down to 13nm achieved
  - Electron-beam + optical lithography

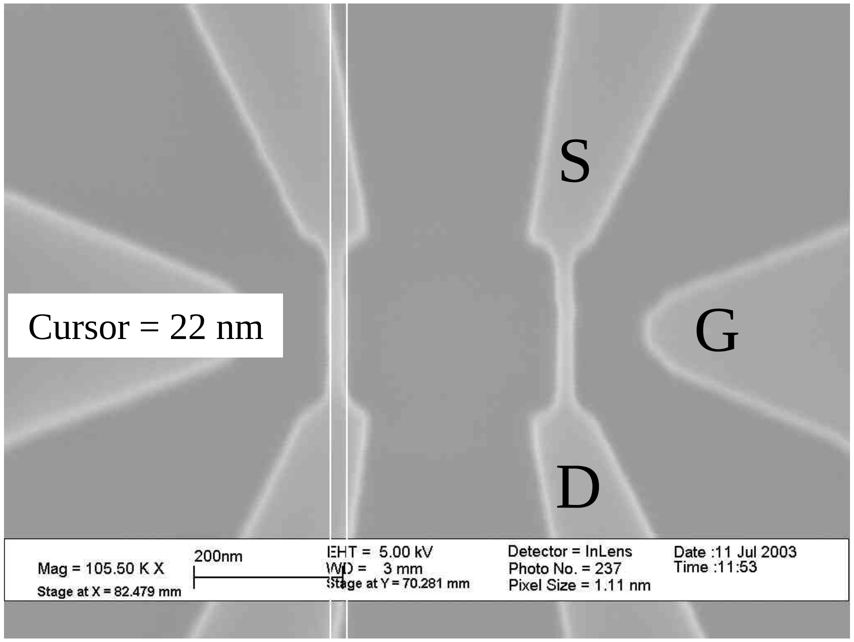




Leland Chang, Patrick Xuan, Prof. Tsu-Jae King UCB

Quantum Computing





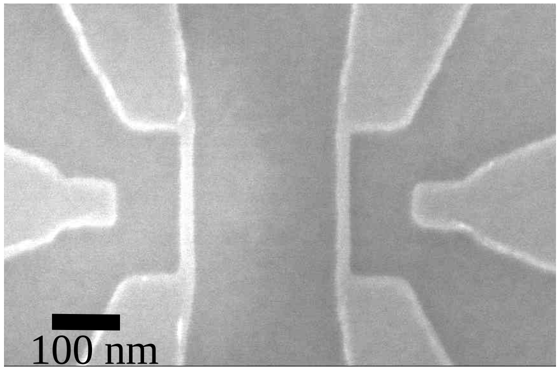
Solid-state quantum computer integrable with Si technology –

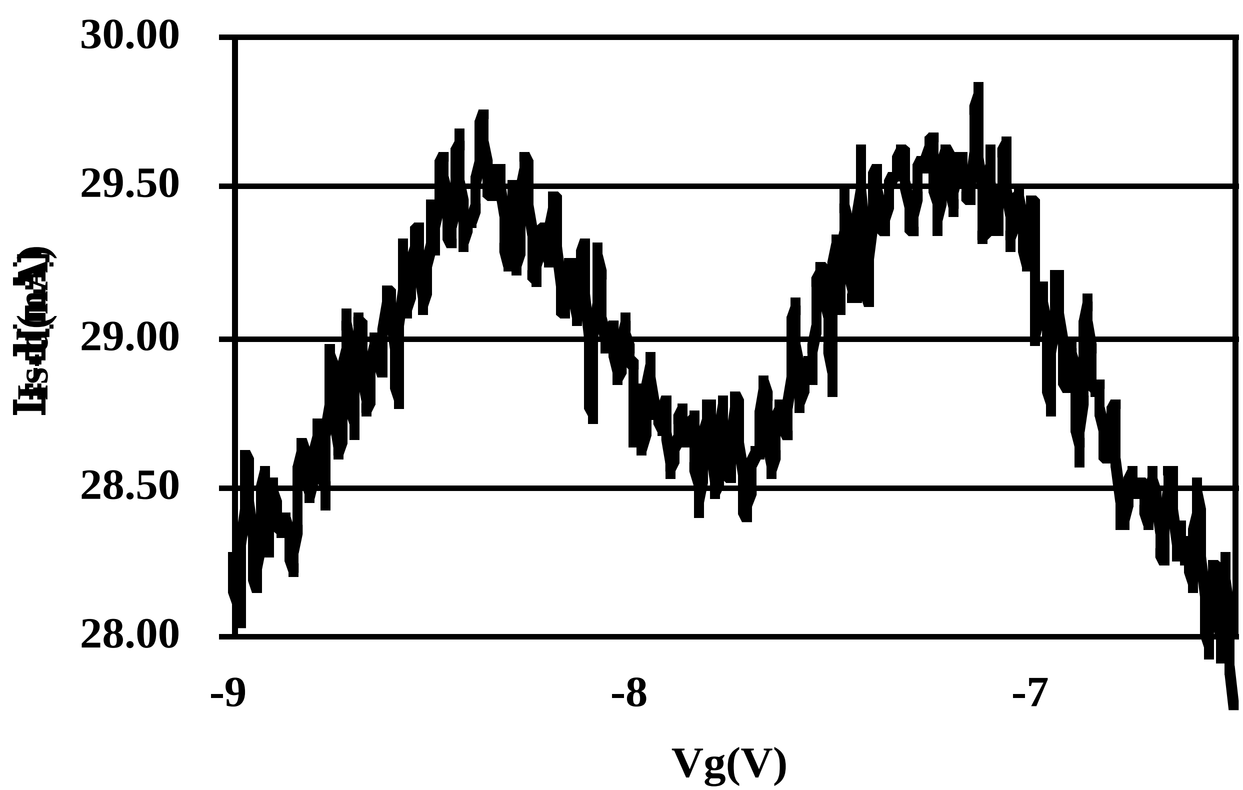
- Integration of ^{31}P qubits with gates to control electron spins and SET readout structures
  - Single ion implantation
  - Electron beam lithography
  - Semiconductor processing

Dr. T. Schenkel, AFRD and Prof. J. Bokor, UCB

S.-J. Park, A. Persaud, J. A. Liddle, J. Nilsson, J. Bokor,
D. H. Schneider, I. Rangelow & T. Schenkel, to appear in MNE 2003

SET Initial Results

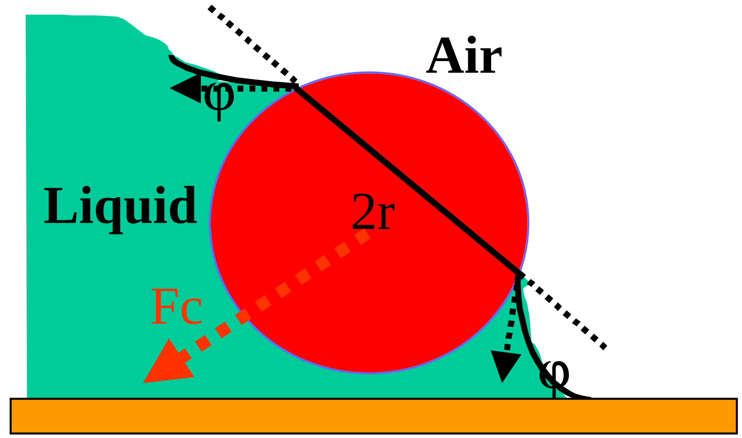




Initial SET measurements show characteristic Coulomb blockade behaviour – inherent noise can be mitigated using dual-RF SET measurement scheme

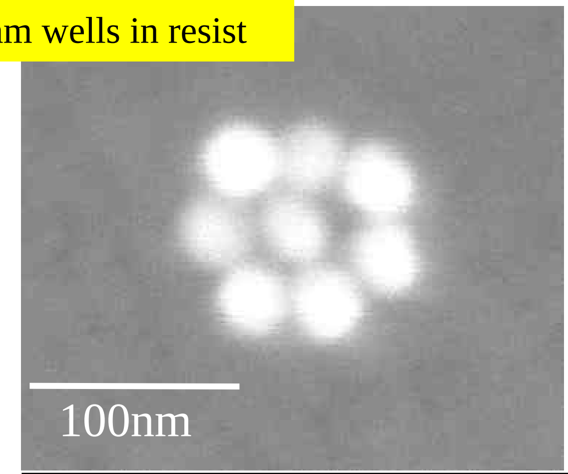
Nanocrystal Assembly

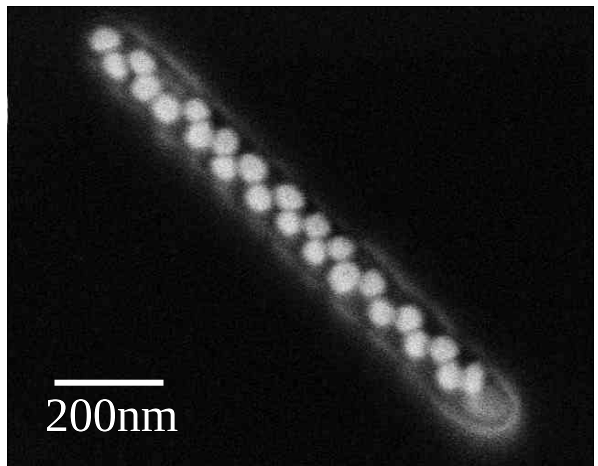
- Nanoparticles must be assembled in a controlled fashion in order to exploit their unique properties fully
  - Microfluidics combined with nanolithography enables accurate placement of nanocrystals

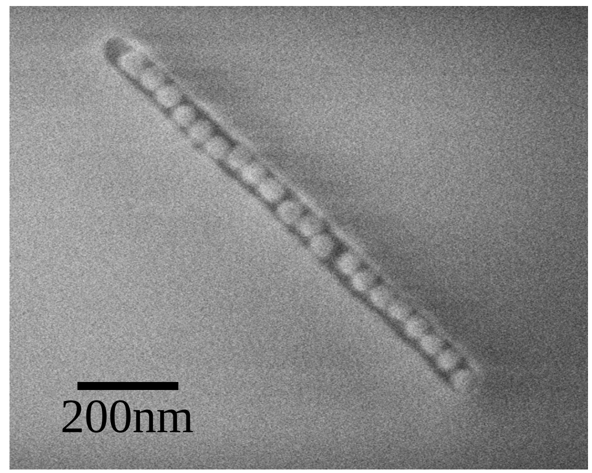


Capillary force, $F_c = 2\pi r\,\sigma\,\sin\varphi$

30 nm Au particles assembled into 100 nm wells in resist

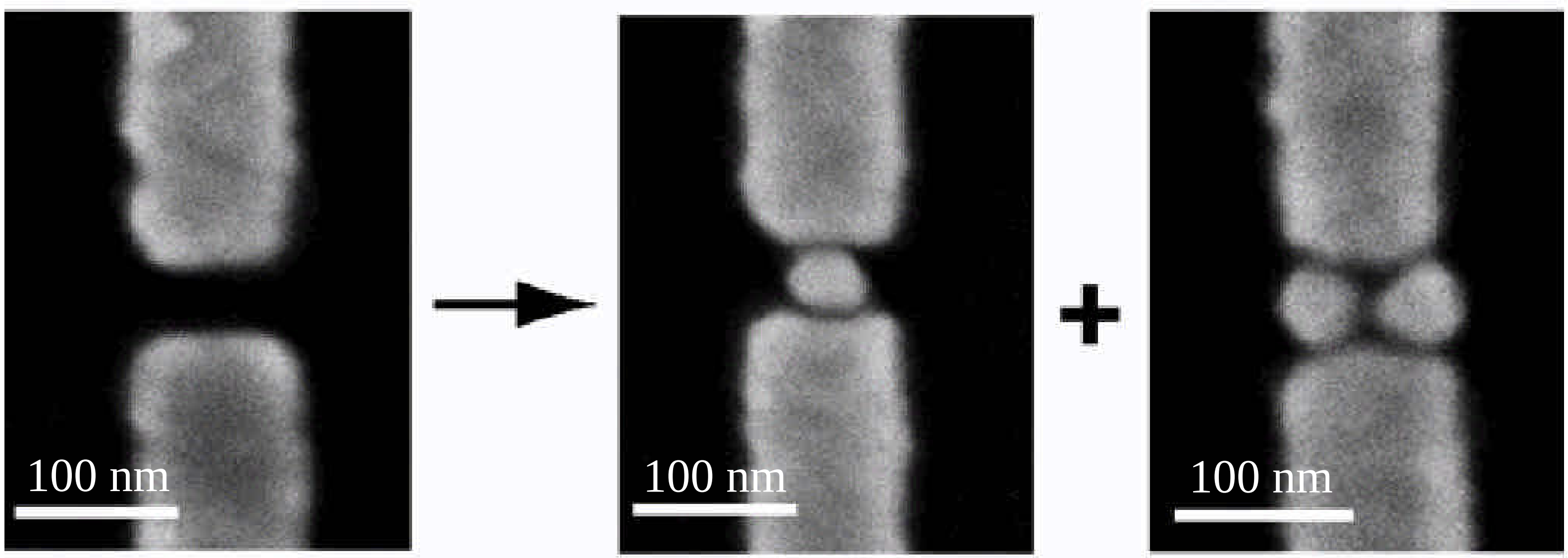




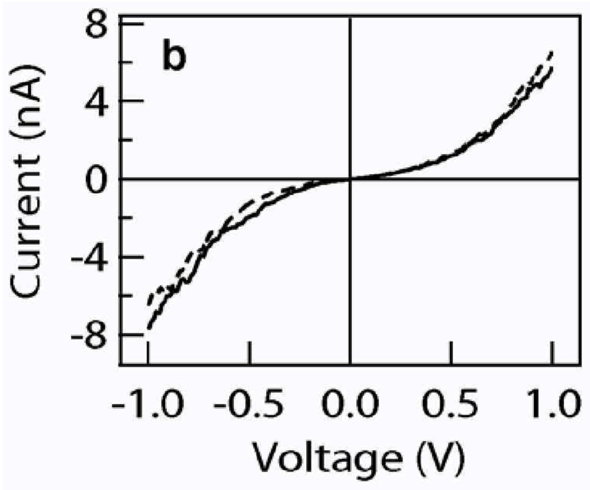


Dr. Yi Cui, Prof. P. Alivisatos, UCB

Electrical Measurements of Nanocrystals



50 nm Au particles assembled between electrodes using capillary forces



Catalysis

Nanoparticle Electrocatalysts

- Perhaps the first industrialized nanotechnology
- 2-10 nm particles dispersed on high surface area support such as carbon (30-100 nm) or carbon nanotubes
- Catalyst dispersion: 30-50 m^2/g_{Pt}
- Fraction of catalyst atoms on surface: 10-40%
- Future direction 30→120 m^2/g_{Pt}, which translates to ~30 g_{Pt}/100 kW_e

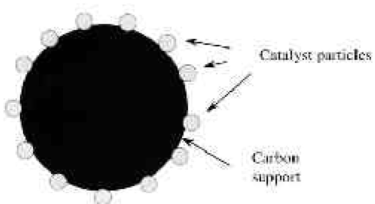
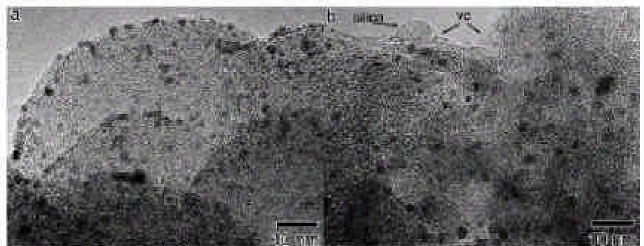
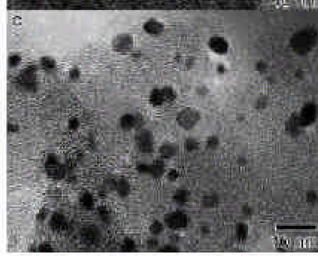
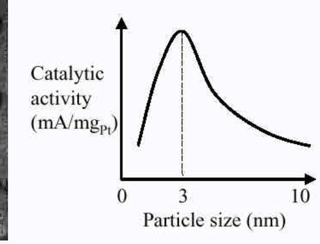


Figure 4.6 The structure, idealised, of a carbon supported platinum catalyst.

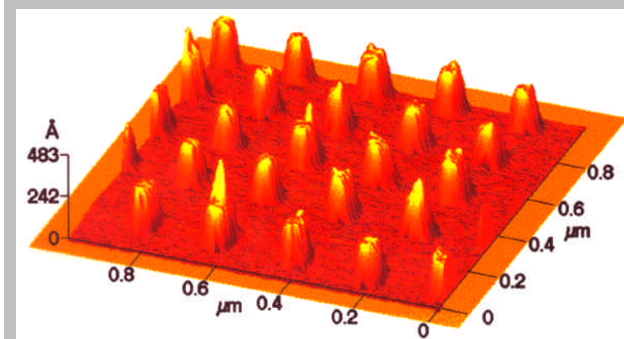






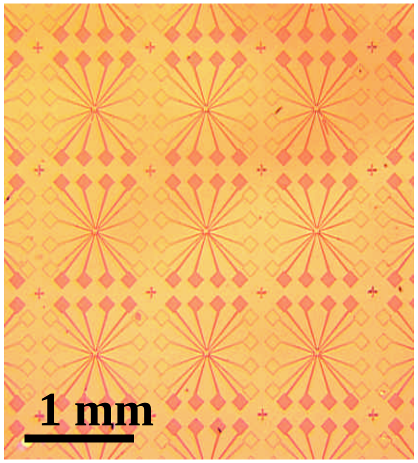
Chao- Yang Wang, Jim Adair, PennState, URL: mtrl1. me. psu. edu

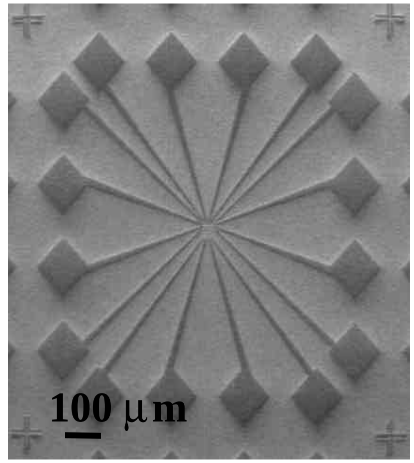
Programmed catalyst distribution for kinetics studies

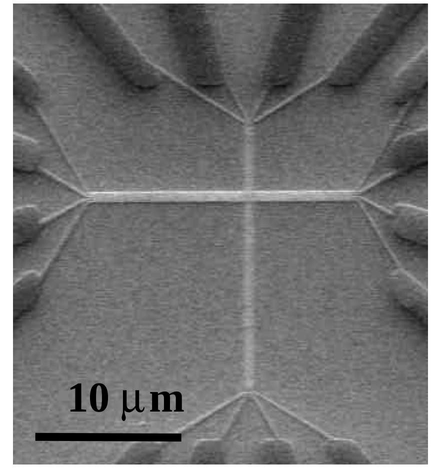


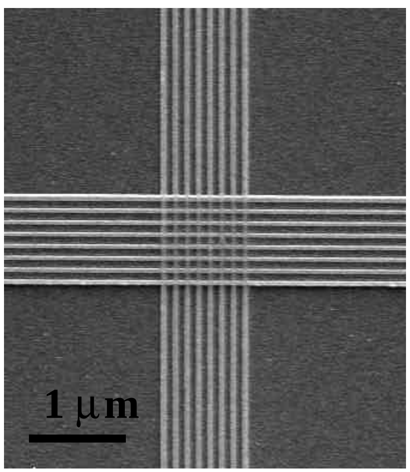
G.A. Somorjai, et al.

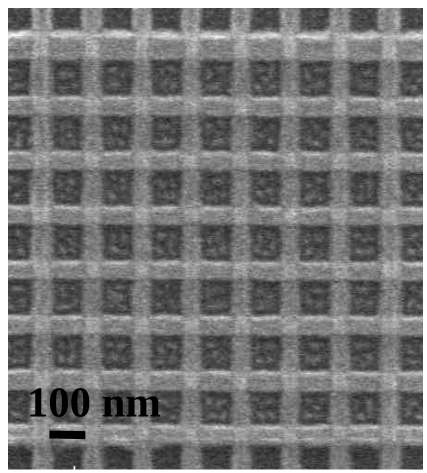
HP/LBNL Nanoimprint Mask for Molecular Electronics

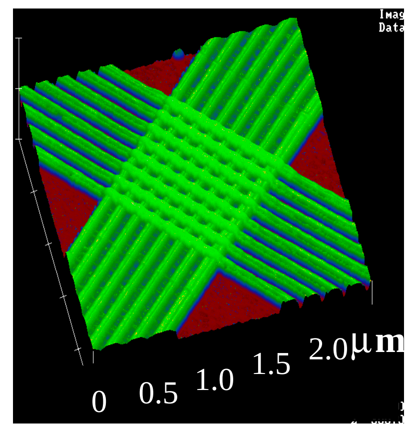








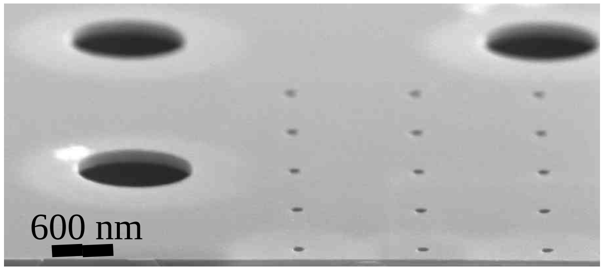


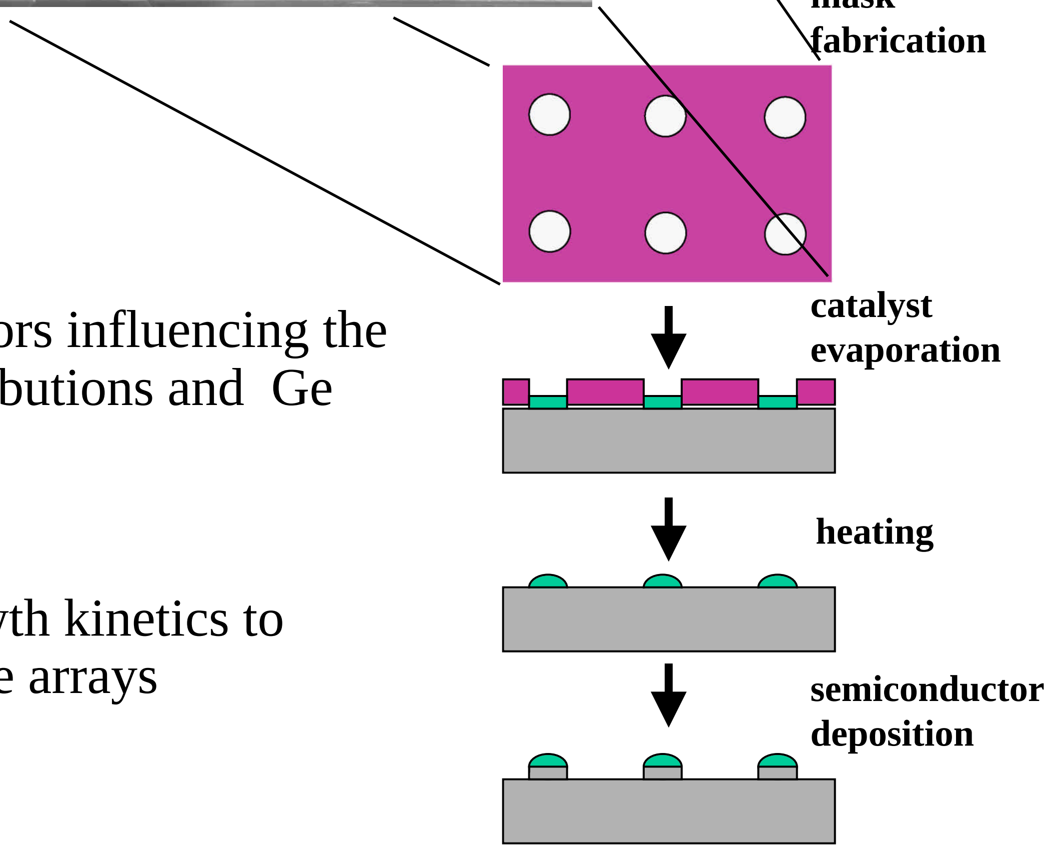


Lines formed by using bilayer as mask for HBr etching of Si

Erik H. Anderson, Deirdre Olynick, Bruce Harteneck, LBNL, Y. Chen H.P./UCLA

Nanocrystal Catalyst Formation

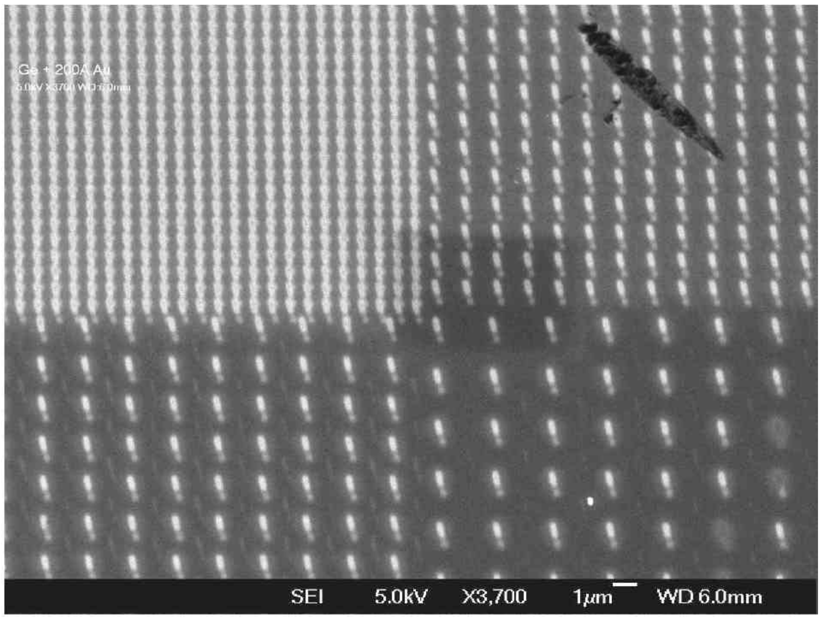




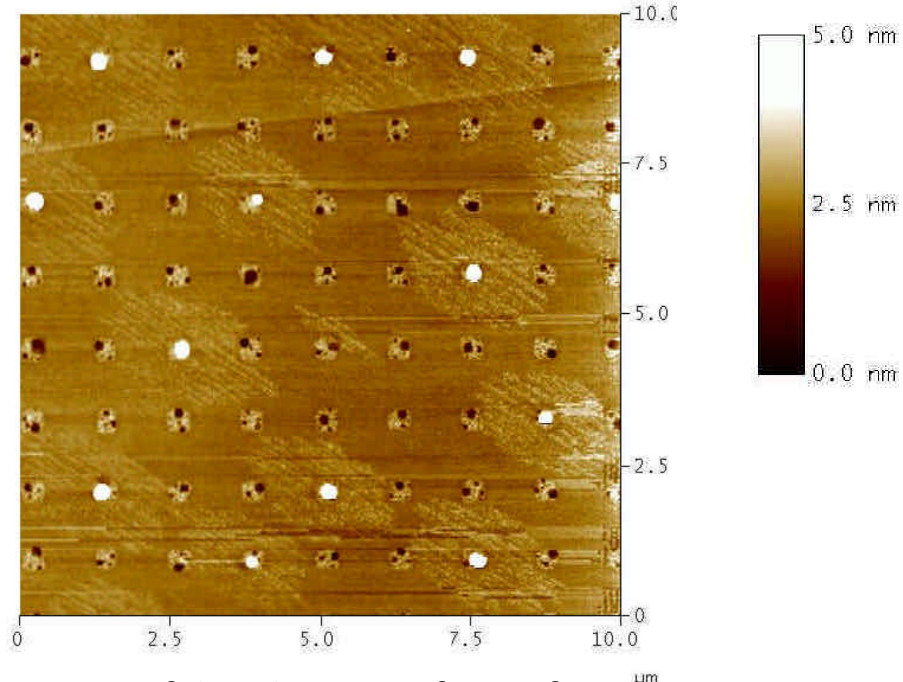
- Fabricate nanoscale patterns of Au to catalyze the growth of nanoscale Ge-island arrays
  - Determine the experimental factors influencing the stability of growth-catalyst distributions and Ge island morphology
  - Understand and manipulate growth kinetics to realize a variety of nanostructure arrays

Jeremy Robinson, Prof. O. Dubon, UCB

Au-catalyzed growth: initial results



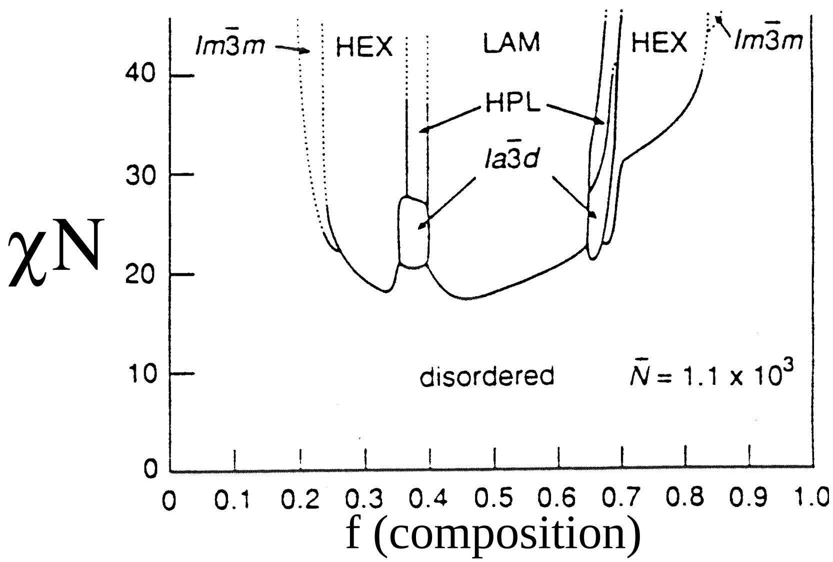
Au dots evaporated through stencil mask onto Ge surface

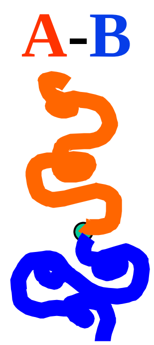


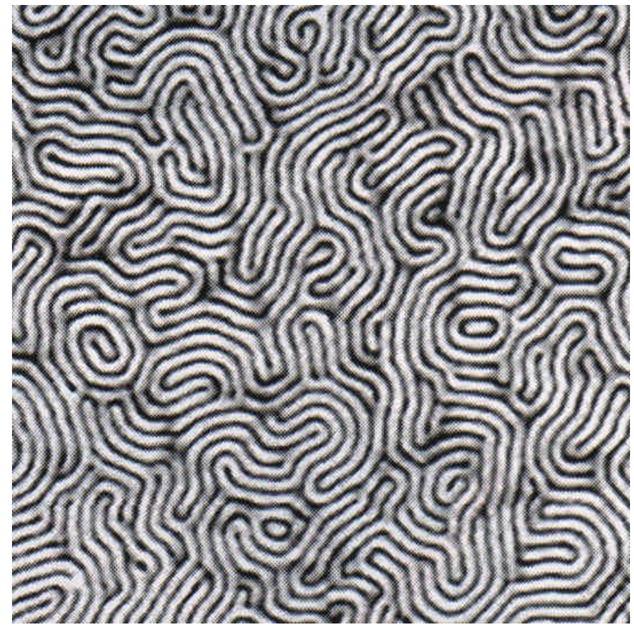
AFM of (100) Ge surface after deposition of 20 Å Au and 600 °C anneal

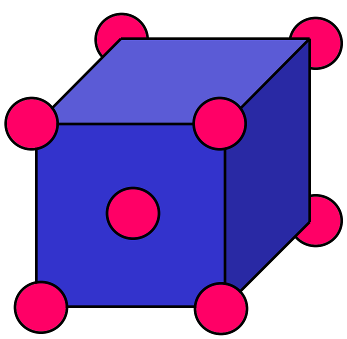
Diblock copolymers

Nitash Balsara, UCB, Paul Nealey, UWI

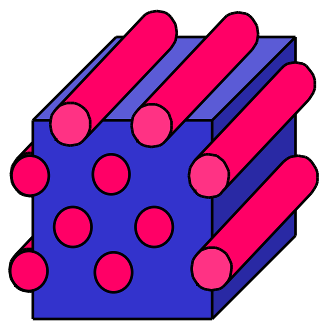




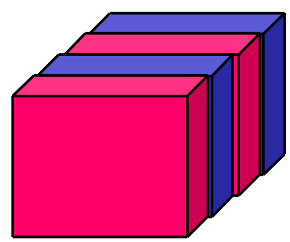




Body-centered cubic

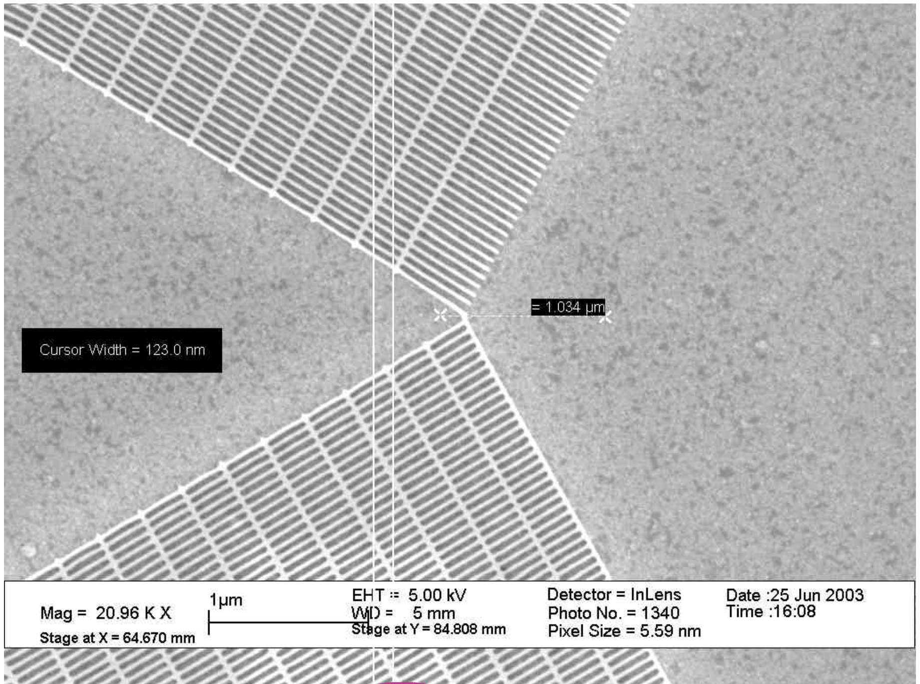


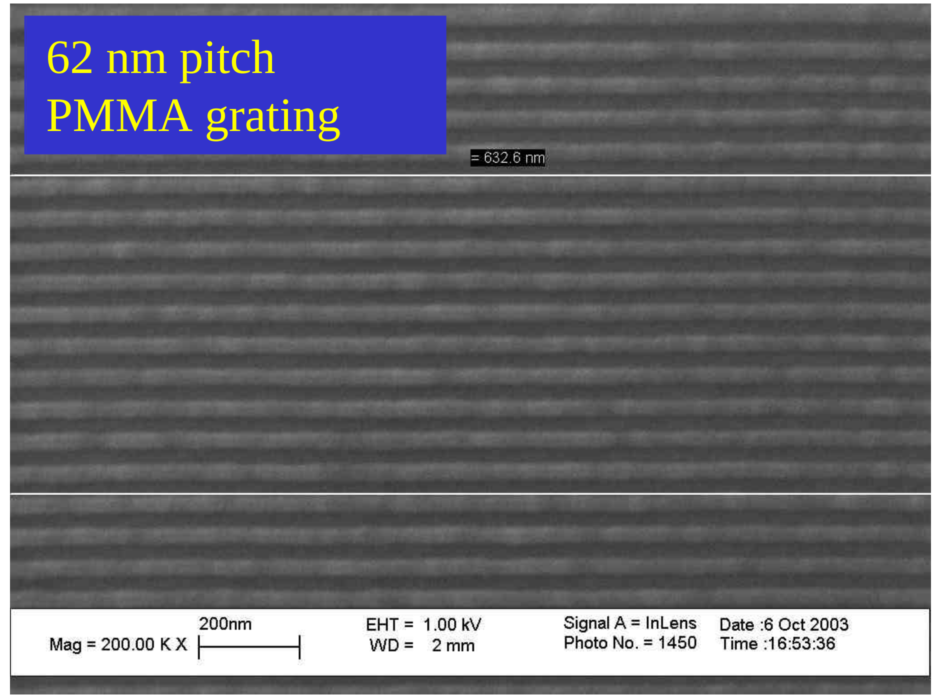
Hexagonal

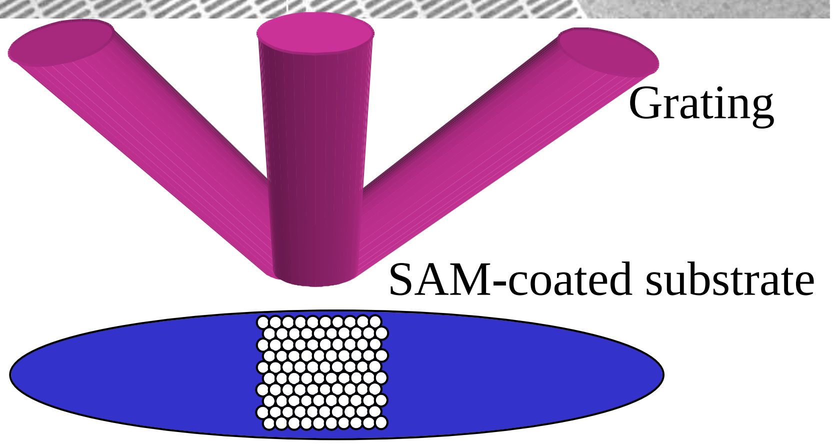


Lamellar

EUV Interferometric Lithography for Guided Self-Assembly



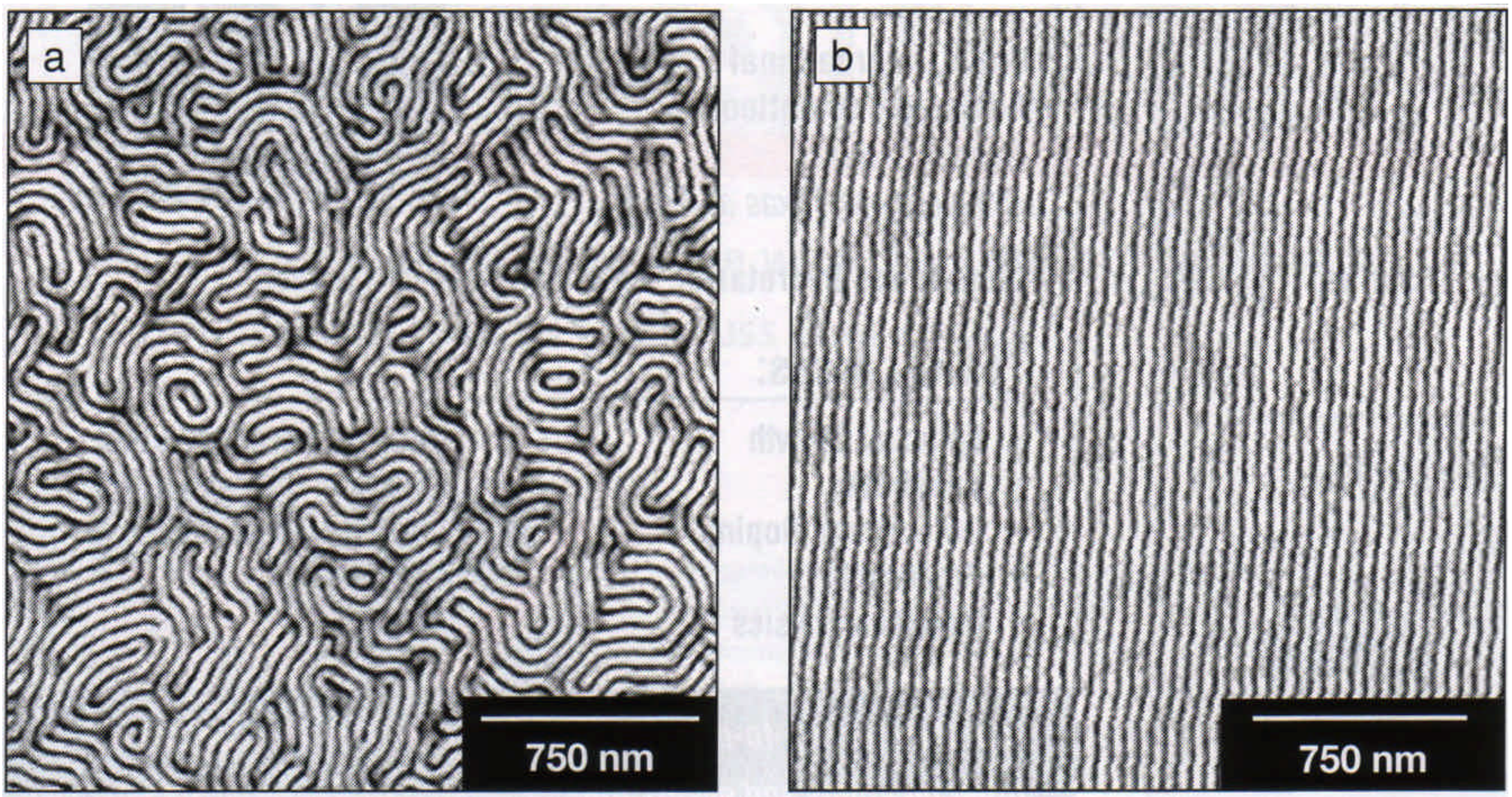




- Interferometric lithography using EUV is used to chemically pattern materials at the nanoscale
  - Di-block copolymer phases show preferential attachment to pattern

Prof. Paul Nealey, U. Wisconsin, Madison

Guided Diblock Copolymer

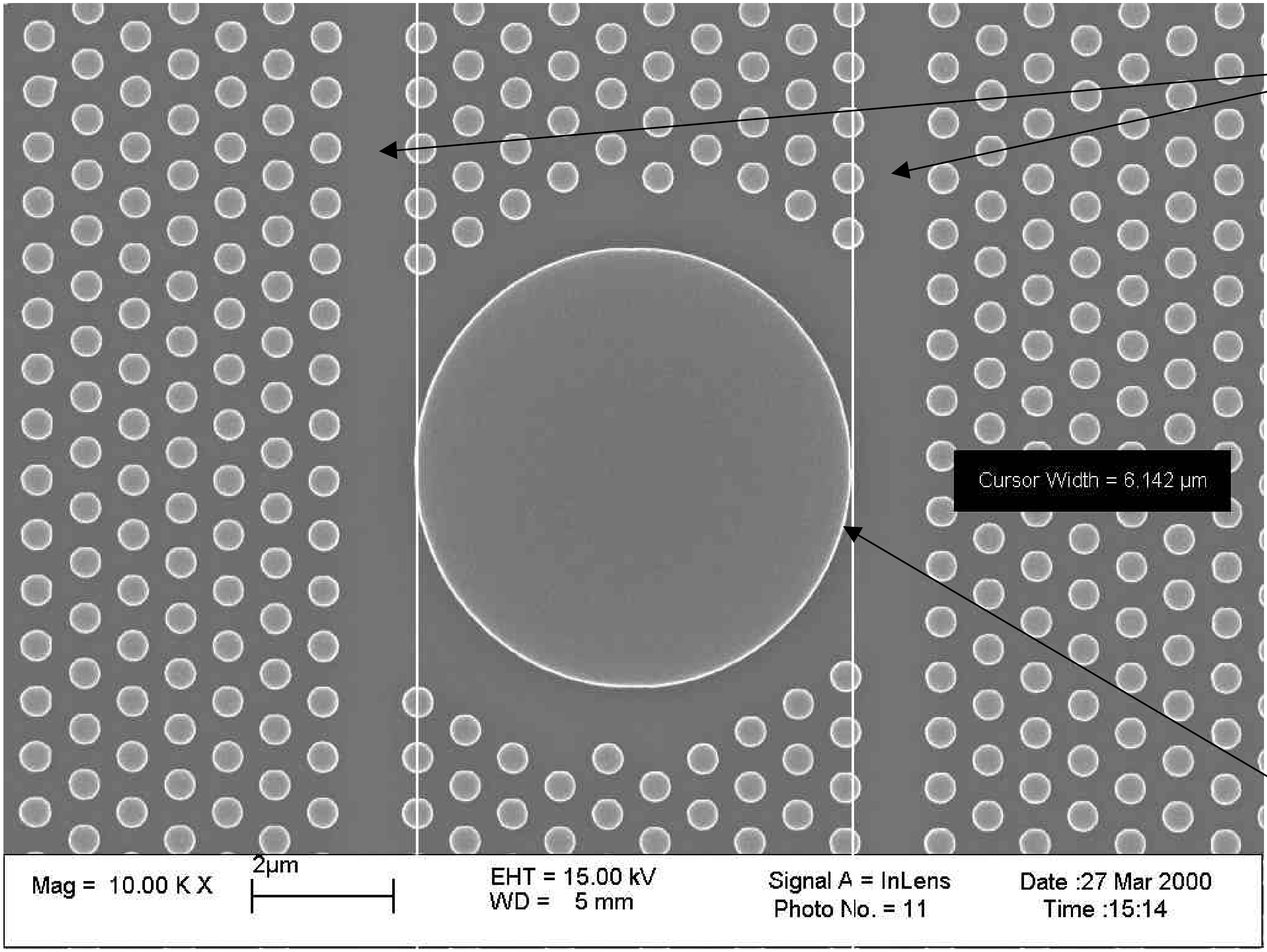


Without chemically patterned substrate

With chemically patterned substrate

P. Nealey, U. Wisconsin, Madison

Photonic Crystal Coupler: KRS



Waveguides

Lattice (Placement & CD control critical)

Resonator (CD control critical)